REMARKS

The following remarks are made in response to the Non-Final Office Action mailed June 25, 2007. Claims 1-38 were rejected. Claims 1-38 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 102

The Examiner rejected claims 1-3, 17, 18, and 31 under 35 U.S.C. § 102(b) as being anticipated by Usami, U.S. Patent No. 6,205,516 ("Usami").

Applicant submits that Usami fails to teach or suggest the limitations recited by independent claim 1 including **a bypass circuit configured to receive the data from the array of memory cells and to bypass the memory; and a circuit configured to select between receiving the data from the memory to provide first output signals and receiving the data from the bypass circuit to provide second output signals based on a column address strobe latency select signal.**

Usami discloses that each SDRAM includes a DRAM core 37. The DRAM core 37 is constructed from a plurality of banks. The SDRAM further includes a clock buffer 30, a command decoder 31, an address buffer/register and bank select 32, a pair of control signal latches 34, a mode register 35, a pair of column address counters 36, and an I/O data buffer/register 33. (Col. 7, line 64 - col. 8, line 3). The I/O data buffer/register 33 serves as a buffer circuit or register circuit for temporarily storing data to be written to the DRAM core 37 or for temporarily storing data read from the DRAM core 37. The I/O data buffer/register 33 is connected to the corresponding data bus "I/O data DQ0-DQ3" that is connected to the CPU 1. (Col. 9, lines 62 - col. 10, line 1).

The Examiner submits "SDRAM is inherently created from a memory array, a memory configured to receive data from the array, a bypass circuit, and a circuit that will select the programmed mode. Figure 4 shows that depending on the contents of the CAS Latency bits A4, A5, and A6 the CL (CAS latency) will vary accordingly as described in Claims 2 and 3. Cache Latencies are varied by changing the number of pipeline stages in the cache. A CL of one means that a cache has one pipeline stage, a CL of two means two pipeline stages, and so on. Therefore, in providing multiple CLs Usami inherently teaches bypassing one or more pipeline

stages based on setting of the CAS Latency bits. In bypassing a pipeline stage, a bypass circuit and a circuit configured to select between receiving data are inherent." (Office Action, page 4).

Applicant submits that it is not inherent in Usami that a bypass circuit is used as recited in claim 1. As the Federal Circuit has stated, "[i]nherent anticipation requires that the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art." *Trintec Indus., v. Top-U.S.A. Corp.*, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002) (quoting *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Since varying the CAS latency in Usami could be performed without utilizing a bypass circuit as recited in claim 1, the limitations of claim 1 are not inherent in Usami as submitted by the Examiner. In addition, there is not a single reference to a cache memory including pipeline stages in Usami.

Figures 2 and 4 and the associated text of Usami do not disclose a bypass circuit or a circuit configured to select between receiving the data from the memory array to provide first output signals and receiving the data from the bypass circuit to provide second output signals based on a column address strobe latency select signal as recited in independent claim 1. In contrast, Usami merely discloses an I/O data buffer/register 33 for receiving data from the DRAM core 37 or writing data to the DRAM core 37. Nowhere in the text or figures does Usami disclose a bypass circuit for routing the data around I/O data buffer/register 33 based on a column address strobe latency select signal. There is also no teaching or suggestion that I/O data buffer/register 33 includes pipeline stages. Even if I/O data buffer/register 33 did include pipeline stages, I/O data buffer/register 33 does not receive a CAS latency select signal for selecting a pipeline stage. The CAS latency select signal is only provided to column address counter 36.

The mode register 35 is for extracting operation mode information, such as the CAS latency, the burst type, and the burst length, from the address data A0-A11 when the mode register 35 receives the address data A0-A11 in correspondence with a predetermined "mode register set" command that is received from the command decoder 31. Mode register 35 supplies each column address counter 36 with a control signal designating the burst length, the burst type, and the CAS latency, thereby controlling count up timing and count up number of the column address counter 36. (Col. 9, lines 45-62). Therefore, Usami discloses controlling the CAS

latency based on controlling the column address counter 36, not by using a bypass circuit as recited in claim 1.

In view of the above, Applicant respectfully submits that the above rejection of independent claim 1 under 35 U.S.C. § 102(b) should be withdrawn. Dependent claims 2 and 3 further define patentably distinct independent claim 1. Accordingly, Applicant believes that these dependent claims are also allowable over the cited references. Allowance of claims 1-3 is respectfully requested.

For similar reasons as discussed above with reference to claim 1, Applicant submits that Usami also fails to teach or suggest the limitations recited by independent claim 17 including **a bypass circuit that bypasses the first in/first out memory; and a control circuit configured to provide first signals and second signals, wherein the first signals latch data from the first in/first out memory to provide a column address strobe latency of greater than one and the second signals latch data from the bypass circuit to provide a column address strobe latency of one.**

In view of the above, Applicant respectfully submits that the above rejection of independent claim 17 under 35 U.S.C. § 102(b) should be withdrawn. Dependent claim 18 further defines patentably distinct independent claim 17. Accordingly, Applicant believes that this dependent claim is also allowable over the cited references. Allowance of claims 17 and 18 is respectfully requested.

For similar reasons as discussed above with reference to claim 1, Applicant submits that Usami also fails to teach or suggest the limitations recited by independent claim 31 including **means for receiving the data read from the array of memory cells to bypass the means for storing data; means for retrieving the data from the means for storing the data if column address strobe latency is greater than one; means for retrieving the data from the means for receiving the data if the column address strobe latency is one.**

In view of the above, Applicant respectfully submits that the above rejection of independent claim 31 under 35 U.S.C. § 102(b) should be withdrawn. Allowance of claim 31 is respectfully requested.

~~Claim Rejections under 35 U.S.C. § 103~~

The Examiner rejected claims 4-16, 19-30, and 32-38 under 35 U.S.C. § 103(a) as being unpatentable over Usami.

Dependent claims 4-16, 19-24, 32, and 33 further define patentably distinct independent claim 1, 17, or 31. Accordingly, Applicant believes that these dependent claims are also allowable over the cited references. Allowance of claims 4-16, 19-24, 32, and 33 is respectfully requested.

In addition, Usami fails to teach or suggest **wherein the circuit comprises a multiplexer configured to select between serialized data from the first circuit and serialized data from the second circuit based on the column address strobe latency select signal** as recited by dependent claim 8. There is no teaching or suggestion in Usami of a first circuit to serialize the data from the memory and a second circuit to serialize the data from the bypass circuit. In addition, there is no teaching or suggestion in Usami of a multiplexer, let alone a multiplexer configured to select between data from the first circuit and data from the second circuit based on the CAS latency select signal. In contrast, Usami discloses a single circuit, I/O data buffer register 33, for temporarily storing data to be written to the DRAM core 37 or for temporarily storing data read from the DRAM core 37. (Col. 9, lines 63-66).

The Examiner cites Fetterman et al., U.S. Patent No. 5,553,256 ("Fetterman") and Sharma et al., U.S. Patent No. 5,829,016 ("Sharma") as evidentiary support for teaching these claim limitations. (Office Action, pages 5-6). Fetterman and Sharma, however, both also fail to teach or suggest a first circuit to serialize the data from the memory, a second circuit to serialize the data from the bypass circuit, and a multiplexer configured to select between data from the first circuit and data from the second circuit based on the CAS latency select signal.

For similar reasons as discussed above with reference to claims 1 and 8, Applicant submits that Usami also fails to teach or suggest the limitations recited by independent claim 25 including **a bypass circuit configured to bypass the memory circuit; a first rise/fall circuit configured to receive data from the memory circuit to provide a first output signal; a second rise/fall circuit configured to receive data from the bypass circuit to provide a second output signal; and a multiplexer configured to select between the first output signal and the second output signal based on a column address strobe latency select signal.**

In view of the above, Applicant respectfully submits that the above rejection of independent claim 25 under 35 U.S.C. § 103(a) should be withdrawn. Dependent claims 26-30 further define patentably distinct independent claim 25. Accordingly, Applicant believes that these dependent claims are also allowable over the cited references. Allowance of claims 25-30 is respectfully requested.

For similar reasons as discussed above with reference to claims 1 and 8, Applicant submits that Usami also fails to teach or suggest the limitations recited by independent claim 34 including **initiating a read command on a first edge of a clock cycle; receiving data read from the array of memory cells in a bypass circuit during the clock cycle; and retrieving the data from the bypass circuit during the clock cycle.**

In view of the above, Applicant respectfully submits that the above rejection of independent claim 34 under 35 U.S.C. § 103(a) should be withdrawn. Dependent claims 35-38 further define patentably distinct independent claim 34. Accordingly, Applicant believes that these dependent claims are also allowable over the cited references. Allowance of claims 34-38 is respectfully requested.

The Examiner rejected claims 1-38 under 35 U.S.C. § 103(a) as being unpatentable over Usami and further in view of Sakamoto et al, "A Digitally Programmable Delay Chip with Picosecond Resolution" ("Sakamoto").

For similar reasons as discussed above with reference to claims 1-38 and for additional reasons discussed below, Applicant submits that Usami and Sakamoto, either alone, or in combination, fail to teach or suggest the limitations recited by claims 1-38.

The Examiner states that "[f]or the purposes of the following rejection Usami fails to disclose a bypass circuit:" (Office Action, page 7). The Examiner also states "[f]igure 1 shows delay circuitry that receives an input and will then delay the data by use of a chain of multiple buffers. As previously stated, if CL-3 then it will need to be delayed three pipeline stages. This will happen by use of the delay circuit. The input will go into the 32 to 1 multiplexer and through the delay chain of buffers as necessary until the desired delay is achieved. However, when CL-1 is selected there can be no delay. The input will go into the 32 to 1 multiplexer and

will immediately be outputted. Therefore at the very least the delay chain of buffers will be bypassed." (Office action, pages 9-10).

Sakamoto, however, does not disclose a *bypass circuit*. As shown in Figure 1 of Sakamoto, the input signals IN and INB pass through a first delay buffer before they are input to input (0) of the 32 to 1 multiplexer. Therefore, the output of the 32 to 1 multiplexer must be delayed, as is the purpose of the delay circuit. Sakamoto does not disclose that the input will go into the 32 to 1 multiplexer and will immediately be outputted as suggested by the Examiner. The delay circuit of Sakamoto does not include a bypass option. The delay buffers cannot be bypassed in the delay circuit of Sakamoto as suggested by the Examiner. The Examiner states that when CL-1 is selected there can be no delay, but as illustrated in Figure 3 of Sakamoto, the minimum delay of the delay circuit is about 1900 ps.

Further the Examiner submits it would have been obvious to utilize the delay circuitry of Sakamoto as the counter delay in Usami. (Office Action, page 10). Usami does not disclose any counter delay. Usami only discloses a column address counter 36 and an I/O data buffer/register 33. One skilled in the art could not combine the delay circuitry of Sakamoto with the device of Usami to provide a *bypass circuit* as recited by the claims.

In view of the above, Applicant submits that the above rejection of claims 1-38 under 35 U.S.C. § 103(a) should be withdrawn. Allowance of claims 1-38 is respectfully requested.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-38 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-38 is respectfully requested.

No fees are required under 37 C.F.R. 1.16(b)(c). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-0471.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to Mark A. Peterson, Telephone No. (612) 573-0120, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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